In re Patent Application of:
MORIN ET AL.
Serial No. 10/701,165
Filing Date: November 4, 2003

REMARKS

Applicants appreciate the Examiner's careful and thorough examination of the present application. By this amendment, independent Claims 12 and 32 have been amended to more clearly define the present invention, and Claims 15-18 and 20-31 have been cancelled. Claims 12-14, 19 and 32-38 remain pending in the application. Favorable reconsideration is respectfully requested.

I. The Claimed Invention

With reference to FIG. 3, for example, the invention of Claims 12 and 32 is directed to a semiconductor device, or method of making, having PMOS and NMOS transistors, so that the residual stress level of an etch-stop layer is discriminately adapted to the type of transistors that it covers. The claims include a first etch-stop layer covering at least one PMOS transistor, and a second etch-stop layer covering the at least one PMOS transistor and at least one NMOS transistor. The first etch-stop layer has a negative residual stress level above the at least one PMOS transistor, and the second etch-stop layer has a positive residual stress level above the at least one NMOS transistor.

II. The Claims are Patentable

Claims 12-38 were rejected in view of Saitoh (US Publication No. 2003/0040158), taken alone or in combination with Zheng (U.S. Patent No. 6,762,085) for the reasons set forth on pages 2-10 of the Office Action. As mentioned above, independent Claims 12 and 32 were amended, and Claims 15-18

and 20-31 were cancelled. Applicants contend that Claims 12-14, 19 and 32-38 clearly define over the cited references, and in view of the following remarks, favorable reconsideration of the rejections under 35 U.S.C. §102 and §103 is requested.

The amended claims now recite that the first etch-stop layer covers the PMOS transistor, and the second etch-stop layer covers both the PMOS transistor and the NMOS transistor. The first etch-stop layer has a negative residual stress level above the PMOS transistor, and the second etch-stop layer has a positive residual stress level above the NMOS transistor. It is this combination of features which is not fairly taught or suggested in the cited references and which patentably defines over the cited references.

As discussed in the present application, increasing the stress leads to an improvement in the performance of an NMOS transistor and a decrease in the performance of a PMOS transistor. Conversely, the use of a material having a negative stress level, i.e., a compressive material, is accompanied by a decrease in the performance of an NMOS transistor and an improvement in the performance of a PMOS transistor.

The Saitoh patent publication is directed to a semiconductor device, and is concerned with the electron mobility in the n-channel MOSFET and reducing the bend or warp of the semiconductor substrate or wafer. Referring to FIG. 5, for example, the first nitride layer 14 has a tensile stress (positive residual stress) and is formed on the substrate to cover the n-channel MOSFET. The tensile stress of the first nitride layer serves to relax a compressive stress existing in

the channel region. The second nitride layer 16 has an actual compressive stress (negative residual stress) and is formed on the substrate to cover both MOSFETs. The first and second nitride layers serve to decrease bend or warp of the substrate.

Accordingly, the Saitoh reference does not teach the use of a first etch-stop layer covering the PMOS transistor, and a second etch-stop layer covering both the PMOS transistor and the NMOS transistor, with the first etch-stop layer having a negative residual stress level above the PMOS transistor, and the second etch-stop layer having a positive residual stress level above the NMOS transistor.

The Zheng et al. patent relates to a method of fabricating a CMOS device with reduced processing costs as a result of a reduction in photolithographic masking procedures. The device includes NMOS and PMOS regions and a silicon nitride layer. This reference does not teach the use of a first etch-stop layer and a second etch-stop layer at all, much less etch-stop layers including the residual stress levels as claimed. Thus, the Zheng et al. reference cannot make up for the deficiencies of Saitoh as set forth above.

There is simply no teaching or suggestion in the cited references to provide the combination of features as claimed. Accordingly, for at least the reasons given above, Applicants maintain that the cited references do not disclose or fairly suggest the invention as set forth in Claims 12 and 32. Furthermore, no proper modification of the teachings of these references could result in the invention as claimed. Thus, the rejections under 35 U.S.C. §102(e) and §103(a) should be withdrawn.

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It is submitted that the independent claims are patentable over the prior art. In view of the patentability of the independent claims, it is submitted that their dependent claims, which recite yet further distinguishing features are also patentable over the cited references for at least the reasons set forth above. Accordingly, these dependent claims require no further discussion herein.

III. Conclusion

In view of the foregoing remarks, it is respectfully submitted that the present application is in condition for allowance. An early notice thereof is earnestly solicited. If, after reviewing this Response, there are any remaining informalities which need to be resolved before the application can be passed to issue, the Examiner is invited and respectfully requested to contact the undersigned by telephone to resolve such informalities.

Respectfully submitted,

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